REMARKS

Claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 are pending in the present application. Claims 1-39 were presented for examination. Claims 1, 8, 14, 19, 26, and 31 have been cancelled by amendment.

In the office action mailed December 13, 2002 ("the Office Action") claims 1-18 and 31-39 were rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 5,357,621 to Cox ("the Cox patent"). Claims 19-30 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Cox patent in view of U.S. Patent No. 6,252,612 to Jeddeloh ("the Jeddeloh patent").

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the present invention are directed to a memory system that allows faulty blocks of memory to be ignored during memory access and enable the otherwise functional memory blocks of the memory to be used. In a particular embodiment, the memory system is implemented in a graphics processing system, and the memory is in the form of embedded memory. Thus, the memory system allows an otherwise functional graphics processing system having faulty blocks of memory to still be used for graphics processing based on the remaining functional blocks of memory.

As described in the present application, for the particular embodiment of the present invention represented in Figures 3a-c, the memory controller 216 includes register 304 having fields 312, 316, 320, 324, and 330, and the embedded memory 220 includes an embedded memory array 308 segmented into four memory blocks 334, 338, 342, and 346. The register 304 includes a memory valid field 312 for storing a value indicative of which memory blocks 334, 338, 342, and 346, are functional, and further includes four BANK fields, 316, 320, 324, and 330. Each field corresponds to one of the four blocks of memory 334, 338, 342, and 346. When the memory is accessed, the values stored in the register 304 are referenced to access the corresponding physical memory location of the memory blocks 334, 338, 342, 346.

Another embodiment of the present invention is described with respect to Figure 5 of the present application.

The memory subsystem 500 has a distributed memory controller arrangement that is represented by registers 504 and 554. Each of the registers 504 and 554 are located in a respective memory controller. As shown in Figure 5, the memory subsystem 500 includes two memory controllers that are coupled together through a memory controller bus. The memory controller bus allows memory access requests, as well as data, to be passed between the two memory controllers. The memory subsystem 580 further includes addressable memory areas represented by memory arrays 508 and 558. The memory array 508 is segmented into m memory blocks and the memory array 558 is segmented into n memory blocks. The register 504 includes start address field 512, memory size field 514, and memory valid field 516, and a number of BANK fields 518-526. Each of the BANK fields 518-526 corresponds to a memory block in the memory array 508. The register 554 includes start address field 562, memory size field 564, and memory valid field 566, and BANK registers 568-574. Each of the BANK fields 568-574 corresponds to a memory block in the memory array 558. The start address field 512 and memory size field 514 are programmed with the start address and memory size for the memory array 508. These values are referenced by the respective memory controllers in order to determine whether to pass a memory access request it receives to another memory controller in order to access the requested memory location.

The memory valid fields 516 and 566 store a value indicative of the functional memory blocks of the respective memory array. The BANK fields 518-526 and 568-574 store values indicating which blocks of memory will be accessed when a memory access request is made to a respective memory bank. As explained with respect to Figure 3, faulty memory blocks of the memory arrays 508 and 558 may be ignored by the memory controllers 504 and 554 by programming the appropriate values in the memory valid fields 516 and 566, and the BANK fields 518-526 and 568-574.

The Cox patent describes an expandable memory system for a serial network. The memory system includes a central memory system controller and individually addressable memory module controllers serially coupled to the memory system controller through a "memory control link" (MCL). An advantage provided by the expandable memory system, or

"MCL system" (Figure 1), described in the Cox patent is that the total capacity of the memory system can be increased or changed by plugging in or removing memory module cards, and the memory system automatically assigns the addresses and memory block positions of the modules in the total memory space without user intervention or the need to physically reposition toggle or slide switches. This is accomplished through the use of the memory system controller communicating with the memory module controller of each memory module via the MCL.

As described in the Cox patent, "the MCL system 10 is used only to interrogate and configure the memory modules 20, and is not used during real time memory accesses by the host system." Col. 4, lines 62-65. The interrogation and configuration process occurs only at start-up, at which time, the memory system controller interrogates the memory modules (*i.e.*, the memory module controller for each memory module) for its memory size and type and assigns a starting address for each of the memory modules. A more detailed description of the interrogation and configuration of the memory modules is provided at col. 5, lines 3-44.

After the interrogation and configuration process is completed, the memory system operates in a conventional manner with little interaction by the MCL controllers 22. That is, memory access commands and data are transferred to and from the memory devices in the conventional manner. As shown in Figure 2, each of the memory blocks 23, 25, 27, and 29 are coupled to a data bus 32, an address bus 28, and a RAS signal line 26 so that each of the memory blocks can be accessed accordingly by the system DRAM controller. A CAS signal line 37A is provided to a memory block control logic 21 for the selection of which memory block 23, 25, 27, or 29 will be activated. The selection of which memory block is based on the address assigned to the memory module 20 by the memory system controller 11.

As shown in Figures 1 and 2, the MCL system 10, that is, the memory system controller, the MCL, and the memory module controller of each memory module, is provided for the limited purpose of memory space allocation. None of the elements have access to data stored by the addressable memory address space, nor do they receive memory access requests. For example, the MCL, which essentially consists of control lines 18a-c, and reset line 16, is limited to serial communication of configuration data from the system controller 11 to the MCL controller 22 of each memory module 20. The MCL is not designed to transfer memory access requests or data. Moreover, the data bus 32 and the MCL controller are not coupled in any

manner, which clearly indicates that the MCL controllers never handle any data during a memory access operation.

As previously mentioned, claims 1-18 and 31-39 were rejected under 35 U.S.C. 102(a) as being anticipated by the Cox patent.

Claim 4 is patentably distinct from the Cox patent. Claim 4 recites a memory subsystem, comprising a first memory array segmented into a plurality of memory sub-arrays having at least one functional memory sub-array, each of the functional memory sub-arrays being assigned to a respective block of memory and any faulty memory sub-arrays being left unassigned, a first memory controller coupled to receive memory access requests to a block of memory to which a functional memory sub-array from the first memory array is assigned and further coupled to the first memory array to access the functional memory sub-array assigned to the requested block of memory, a second memory array segmented into a plurality of memory sub-arrays, a number of which are functional, each of the functional memory sub-arrays of the second memory array assigned to a respective block of memory and any faulty memory sub-arrays left unassigned, a second memory controller coupled to receive memory access requests to a block of memory to which a functional memory sub-array of the second memory array is assigned and further coupled to the second memory array to access the functional memory sub-array assigned to the requested block of memory, and a memory controller bus coupled between the first and second memory controllers to pass a memory access request from one memory controller to the other in response to receiving a memory access request to access a memory location within the memory array coupled to the other memory controller.

The Cox patent fails to describe the combination of limitations recited by claim 4. For example, the Cox patent fails to teach a first memory controller receiving memory access requests to a block of memory to which a functional memory sub-array from the first memory array is assigned in combination with first and second memory controllers coupled together by a memory controller bus on which memory access requests received by one of the memory controllers can be passed to the other memory controller in order to access a memory location in the memory array coupled to that memory controller. As previously discussed, the Cox patent describes a memory system having MCL controllers of each module coupled in a serial fashion for the limited purpose of allocating a total memory space. The MCL controllers are configured

by a memory system controller that assigns base addresses to the memory modules. Once the address space is configured by the memory system controller, the memory system of the Cox system is operated in a conventional manner. None of the MCL controllers handle memory access requests or data, or forwards the same to another MCL controller. The memory banks are coupled directly to common command, address, and data busses over which memory access requests are received by the memory banks directly from the DRAM controller 33. For the foregoing reasons, claim 4 is patentably distinct from the Cox patent.

Claims 10 and 16 were also rejected under 35 U.S.C. 102(a) as being anticipated by the Cox patent. Claim 10 recites, in pertinent part, a memory subsystem receiving memory access requests, comprising a first memory array segmented into a plurality of memory sub-arrays having at least one functional memory sub-array, a first register to store pointer values directing access to each functional sub-array, a first memory controller coupled to the first memory array and the first register to consult the pointer values and determine which functional memory sub-arrays to access in response to receiving the memory access requests, a second memory array segmented into a plurality of memory sub-arrays, a number of which are functional, a second register to store second pointer values directing access to each functional sub-array of the second memory array, a second memory controller coupled to the second memory array and the second register to consult the pointer values and determine which of the memory sub-arrays of the second memory array to access in response to receiving the memory access requests, and a memory controller bus coupled between the first and second memory controllers to pass the memory access request to the other memory controller when the memory access request is to a memory location in the other memory array.

Claim 16 recites a memory subsystem, comprising a memory array segmented into a plurality of memory sub-arrays, a memory controller coupled to access the memory array and having a register including a plurality of data fields, the data fields storing a pointer value indicative of which memory sub-arrays are functional and which memory sub-arrays to access in response to the memory controller receiving a memory access request, a second memory array segmented into a plurality of memory sub-arrays, a second memory controller coupled to access the second memory array and having a register including a plurality of data fields, the data fields of the second memory controller storing a pointer value indicative of which memory sub-arrays

of the second memory array are functional and which to access in response to the second memory controller receiving a memory access request, and a memory controller bus coupled between the memory controller and the second memory controller on which the memory access request may be passed from one memory controller to the other.

The Cox patent fails to teach the combination of limitations recited by claims 10 and 16. As previously discussed with respect to claim 1, the Cox patent does not describe a memory system having the memory controllers coupled to the respective registers to consult pointer values to determine the functional memory sub-arrays in combination with a memory controller bus coupling the memory controllers over which memory access requests received by one of the memory controllers can be passed to the other memory controller. For the foregoing reasons, claims 10 and 16 are is patentably distinct from the Cox patent.

Claims 35 and 37 were also rejected under 35 U.S.C. 102(a) as being anticipated by the Cox patent. Claim 35 recites a method of accessing a memory array segmented into a plurality of memory sub-arrays, at least one of the memory sub-arrays being functional, the method comprising assigning each functional memory sub-array of the memory array to a respective memory block and leaving any faulty memory sub-arrays unassigned, in response to receiving a memory access request to access a particular memory block, accessing the memory sub-array assigned to the particular memory block, storing start address and size values defining an addressable memory area of the memory array, determining from the start address and size values whether the particular memory block of the memory access request is assigned to a memory sub-array within the addressable memory area of the memory array, and servicing the memory access request if the particular memory block is determined to be assigned to a memory sub-array within the addressable memory area of the memory array, otherwise passing the memory access request to another memory controller for servicing.

Claim 37 recites a method of accessing an embedded memory array segmented into a plurality of memory sub-arrays, at least one of the memory sub-arrays being functional, the method comprising storing for each of a plurality of memory blocks a pointer value identifying a functional memory sub-array assigned thereto, storing start address and size values defining an addressable memory area of the embedded memory array, in response to receiving a memory access request to access a particular memory block, determining from the start address

and size values whether the particular memory block is assigned to a memory sub-array within the addressable memory area of the embedded memory array, and accessing the memory sub-array identified by the pointer value stored for the particular memory block if the particular memory block is determined to be assigned to a memory sub-array within the addressable memory area of the embedded memory array, otherwise passing the memory access request to another memory controller for servicing.

The Cox patent fails to teach the combination of limitations recited by claims 35 and 37. For example, the Cox patent does not teach the combination of assigning each functional memory sub-array of the memory array to a respective memory block and leaving any faulty memory sub-arrays unassigned, determining from the start address and size values whether the particular memory block of the memory access request is assigned to a memory sub-array within the addressable memory area of the memory array, and servicing the memory access request if the particular memory block is determined to be assigned to a memory sub-array within the addressable memory area of the memory array, or otherwise passing the memory access request to another memory controller for servicing. For the foregoing reasons, claims 35 and 37 are patentably distinct from the Cox patent.

Claims 4, 10, 16, 35, and 37 are patentably distinct from the Cox patent. Therefore, the rejection of claims 4, 10, 16, 35, and 37 under 35 U.S.C. 102(a) should be withdrawn.

Claims 2, 3, and 5-7, which depend from claim 4, claims 9 and 11-13, which depend from claim 10, claims 15, 17, and 18, which depend from claim 16, claims 32-34, and 36, which depend from claim 35, claims 38 and 39, which depend from claim 37, are similarly patentably distinct from the teachings of the Cox patent based on their dependency from an respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an application represents a different invention, the rejection of an independent claim does not necessarily result in the rejection of claims depending therefrom. For the foregoing reasons, the rejection of claims 2, 3, 5-7, 9, 11-13, 15, 17, 18, 32-34, 36, 38, and 39 under 35 U.S.C. 102(a) should be withdrawn.

As previously mentioned, claims 20-25 and 27-30 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Cox patent in view of the Jeddeloh patent. Claims 22 and 28 are patentable over the Cox patent in view of the Jeddeloh patent because the combined teachings of the references do not teach or suggest the combination of limitations recited by claims 22 and 28.

Claim 22 recites a graphics processing system including a memory subsystem having a first memory array, first memory controller, a second memory array, a second memory controller, and a memory controller bus having the specified operability and limitations recited therein. Claim 28 recites a computer system including graphics processing system with a memory subsystem having a first memory array, a first memory controller a second memory array, a second memory controller, and a memory controller bus having the specified operability and limitations recited therein.

The Examiner has cited the Jeddeloh patent as teaching "a computer, comprising at least one processor; and at least two memory controllers, wherein one of the at least two memory controllers includes an accelerated graphics port and at least one configuration register defining a range of addresses that are available for accelerated graphics port transactions." *See* Office Action, page 7. Without addressing the merits of the Examiner's characterization of the teachings of the Jeddeloh patent, even if it is assumed that the Jeddeloh patent does teach the material as stated by the Examiner, those teachings do not make up for the deficiencies of the Cox patent. As previously discussed with respect to claims 4, 10, 16, 35, and 37, the Cox patent does not teach the combination of memory controllers, memory arrays, and memory controller bus as claimed in claims 22 and 28. The teachings of the Jeddeloh patent, as characterized by the Examiner, do not make up for the teachings Cox.

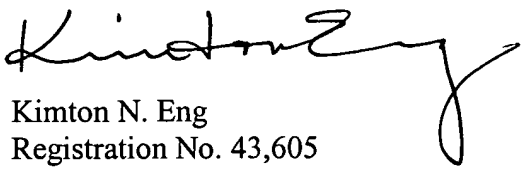
For the foregoing reasons, claims 22 and 28 are patentable over the combined teachings of the Cox patent in view of the Jeddeloh patent. Claims 20, 21, and 23-25, which depend from claim 22, and claims 27, 29, and 30, which depend from claim 28 are also patentable based on their dependency from an allowable base claim. Therefore, the rejection of claims 20-25 and 27-30 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is

requested to contact the undersigned at the number listed below for a telephone interview if, upon consideration of this amendment, the Examiner determines any pending claims are not in condition for allowance. The undersigned also requests the Examiner to direct all future correspondence to the address set forth below in the event the Examiner shows a different correspondence address for the attorney of record.

Respectfully submitted,

DORSEY & WHITNEY LLP



Kimton N. Eng
Registration No. 43,605

KNE:asw

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)
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